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In re Application of:

Hisanori FUJISAWA

Serial No.: 09/045,041 Group Art Unit: 2123

Confirmation No.: 9340 Examiner: H. Jones

Filed: March 20, 1998 Appeal No.:

For: METHOD AND APPARATUS FOR CARRYING OUT CIRCUIT SIMULATION

Assistant Commissioner for Patents
Washington, D.C. 20231

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BRIEF OF APPELLANT

In a Notice of Appeal filed February 26, 2003, the Applicant appealed the Examiner's November 27, 2002 Office Action finally rejecting claims 9-12, 14-24, 26-36, and 38-44. Therefore, Appellant's brief is due April 26, 2003. A Petition for a one-month extension of time is filed herewith, together with the requisite fee for same, thereby extending the due date for response to May 26, 2003. The requisite filing fee as set forth in 37 C.F.R. §1.17(f) is enclosed herewith. Applicant submits this Appeal Brief in triplicate.

1. REAL PARTY IN INTEREST (37 C.F.R. §1.192(c)(1))

The real party in interest is FUJITSU LIMITED, the assignee of the subject application.

2. RELATED APPEALS AND INTERFERENCES ((37 C.F.R. §1.192(c)(2))

Appellant, Appellant's legal representatives, and the assignee are not aware of any other appeals or interferences that will directly affect or be directly affected by, or have a bearing on, the Board's decision in the pending appeal.

3. STATUS OF CLAIMS ((37 C.F.R. §1.192(c)(3))

Appealed claims 9-12, 14-24, 26-36, and 38-44 have been rejected.

4. STATUS OF AMENDMENTS ((37 C.F.R. §1.192(c)(4))

An amendment under 37 C.F.R. § 1.116 was filed February 26, 2003 in response to the November 27, 2002 final Office Action. According to a March 28, 2003 Advisory Action, this amendment will not be entered. All other amendments have been entered.

5. SUMMARY OF INVENTION ((37 C.F.R. §1.192(c)(5))

Referring to Figs. 3, 5, 6, and 8 through 13 of the drawings, the features of the present invention, as set forth in claims 9-12, 14-24, 26-36, and 38-44, are summarized below.

The present invention relates to a circuit simulation method and apparatus for simulating and inspecting a large-scale integrated ("LSI") circuit such as a MOS LSI circuit to satisfy design specifications and improve performance of the circuit. Because a MOS LSI circuit is large in scale, the circuit needs to be simplified while ensuring accuracy of circuit operation. Simplifying the circuit reduces the time required for simulation and enables high-speed simulation.

In the present invention, first, partial circuits (e.g., partial circuits 11 and 12 of Fig. 9) are extracted from the circuit to be simulated and inspected for equivalence (Fig. 5 at S11 and page 19, lines 15-19 of the specification). If the configurations (e.g., types of circuit elements) of the extracted partial circuits are consistent with each other (Fig. 5 at S12), then the operational characteristics of the corresponding circuit elements are compared with each other (Fig. 5 at S13 and page 19, lines 21-33 of the specification). Next, if all pairs of corresponding circuit elements have the same operational characteristics, then the input and output terminals are compared with each other (Fig. 5 at S14 and page 20, lines 1-6 of the specification). If the corresponding input and output terminals are identical, then the operational characteristics of the extracted partial circuits are considered to be equivalent (Fig. 5 at S16 and page 20, lines 8-12 of the specification). Figures 9 and 11 provide examples of circuits having equivalent partial circuits.

However, if the input or output terminals are not identical (e.g., as shown in Figs. 10 and 12), then other partial circuits connected to the input or output terminals of the extracted partial

circuits are inspected for "quasi-equivalence" (Fig. 5 at S15 and page 20, lines 13-20 of the specification). If quasi-equivalence is found, the extracted partial circuits are considered to be equivalent (Fig. 5 at S15 and S16 and page 20, lines 20-26 of the specification). Figures 10 and 12 show examples of circuits having partial circuits that are not equivalent.

For example, in Fig. 9, partial circuit 11 contains PMOS transistors T1 and T5 and NMOS transistor T2. Partial circuit 12 contains PMOS transistors T3 and T6 and NMOS transistor T4. The PMOS and NMOS transistors all have the same configurations and operational characteristics. The corresponding input and output terminals of partial circuits 11 and 12 are identical. Thus, partial circuits 11 and 12 are determined to have equivalent operational characteristics. See page 24, lines 2-11 of the specification.

As another example, in Fig. 10, partial circuit 21 contains PMOS transistors T11 and T15 and NMOS transistor T12. Partial circuit 22 contains PMOS transistors T13 and T16 and NMOS transistor T14. The PMOS and NMOS transistors all have the same configurations and operational characteristics. However, the corresponding output terminals of partial circuits 21 and 22 are connected to different NMOS transistors (i.e., T17 and T18, respectively) and are not identical. Thus, partial circuits 21 and 22 are determined to not have equivalent operational characteristics. See page 24, lines 12-35 of the specification.

Quasi-equivalence is determined by calculating the "intensity of influence" of a terminal external to the extracted partial circuits on terminals of the extracted partial circuits. The intensity of the influence of the external terminal is assessed as the frequency of shifting from the source or drain of a MOS semiconductor device to the gate thereof in the course of tracing a path linking the external terminals and an object terminal. See page 17, lines 6-14 of the specification. In other words, the number of MOS transistors encountered or the number of gate terminals that exist, when tracing an arbitrary path linking the external terminal to the given terminal, is defined as the frequency of shifting of the external terminal with respect to the object terminal.

For example, Fig. 8 illustrates determination of the intensity of influence of external terminal A on the other terminals. For terminal E, the frequency of shifting from the source or drain of a MOS transistor to the gate thereof when tracing a path from terminal A to terminal E is 2. Thus, the intensity of influence on terminal E is 2. See page 23, lines 12-25 of the specification. If the intensity of influence is greater than or equal to a specified value, which means that the influence of the external terminals is negligible, then the partial circuits in

question are considered to be quasi-equivalent circuits that exhibit equivalent operational characteristics (Fig. 6 at S23 and S25 and page 17, lines 14-24 and page 21, lines 17-20 of the specification). Figure 12 illustrates an example of a circuit having partial circuits that are quasi-equivalent.

After the circuit is compressed by integrating the partial circuits exhibiting the equivalent operational characteristics into one circuit, circuit simulation is carried out (Fig. 3 at S4 and page 13, lines 4-8 of the specification). Figure 13 shows a compressed form of the circuit of Fig. 11 (page 26, lines 27-37 of the specification).

In conventional circuit simulation methods, only circuit elements located in a limited area within a circuit can be inspected to determine whether these circuit elements exhibit the same characteristics. An example of a conventional circuit simulation method is provided by referring to Figs. 1(A), 1(B), 2(A), and 2(B). In Fig. 2(A), nets Ni are given identification numbers N1, N2, and N3 (Fig. 1(A) at S200 and S210). Circuit elements interconnected within the same net Ni are inspected for the same characteristics (Fig. 1(A) at S220 and S230). Identical circuit elements are given the same identification number (Fig. 1(A) at S240). For example, NMOS transistor Q1 and NMOS transistor Q2 are considered to be identical circuit elements, and identification number b1 is assigned to both transistors. See page 1, line 11 to page 3, line 21 of the specification.

Next, corresponding terminals of the identical circuit elements are compared (Fig. 1(B) at S245). For example, the electrical conditions for connection of the source, drain, and bulk resistor of NMOS transistor Q1 are compared to those of NMOS transistor Q2. Circuit elements having corresponding terminals with the same characteristics are integrated into one circuit element (Fig. 1(B) at S250 and 260). For example, NMOS transistors Q1 and Q2 of Fig. 2(A) are integrated into NMOS transistor Q1' as shown in Fig. 2(B). See page 3, line 22 to page 4, line 7 of the specification.

In the example shown in Fig. 2(C), NMOS transistor Q10 and NMOS transistor Q20 do not have corresponding terminals with the same characteristics because the source of NMOS transistor Q10 is connected to a source power supply VSS, while the source of NMOS transistor Q20 is connected to the drain of NMOS transistor Q30. See page 4, line 35 to page 5, line 27 of the specification.

Thus, in conventional circuit simulation methods, only circuit elements located in a limited area within a circuit can be inspected to determine whether these circuit elements exhibit the same characteristics, and it is difficult to distinguish all circuit elements exhibiting equivalent operational characteristics in the circuit to be simulated. Thus, the circuit may not be compressed effectively. The present invention provides the ability to easily integrate a plurality of partial circuits in a broader area into one circuit. As a result, a circuit to be simulated can be compressed more effectively, reducing the scale of the circuit and the time required to reduce the circuit.

6. ISSUES ((37 C.F.R. §1.192(c)(6))

A first issue is whether claims 9-12, 14-24, 26-36, and 38-44 are anticipated by Filseth (U.S. Patent No. 5,473,546); or Yokomizo et al. ("A New Circuit Recognition and Reduction Method for Pattern Based Circuit Simulation," IEEE Custom Integrated Cir. Conf., pp. 9.4/1-9.4/4); or Chakrabarti et al. ("An Improved Hierarchical Test Generation Technique for Combinational Circuits with Repetitive Sub-Circuits," IEEE Proc. Test Symp., pp. 237-243); or Hachiya (U.S. Patent No. 6,031,979).

A second issue is whether claims 9-12, 14-24, 26-36, and 38-44 patentably distinguish over Shinsha et al. (U.S. Patent No. 4,882,690); or Wang et al. ("Restructuring Binary Decision Diagrams Based on Functional Equivalence," IEEE Design Automation, pp. 261-65); or Kuehlmann et al. ("Equivalence Checking Using Cuts and Heaps," IEEE Proc. 1997 Design Auto. Conf., pp. 263-68).

A subissue is whether the cited references teach or suggest inspecting a plurality of extracted partial circuits to detect partial circuits exhibiting equivalent operational characteristics, based on the configurations of the plurality of partial circuits, and determining equivalence when the configurations of the plurality of partial circuits are mutually consistent.

Another subissue is whether the cited references teach or suggest compressing the circuit to be simulated by integrating the partial circuits exhibiting equivalent operational characteristics into one circuit and simulating the compressed circuit.

7. GROUPING OF CLAIMS ((37 C.F.R. §1.192(c)(7))

The claims stand or fall together.

8. ARGUMENT ((37 C.F.R. §1.192(c)(8))

Rejections Under § 102

In the final Office action, the Examiner rejected claims 9-12, 14-24, 26-36, and 38-44 under 35 U.S.C. §102(b) as being anticipated by Filseth (U.S. Patent No. 5,473,546); or Yokomizo et al. ("A New Circuit Recognition and Reduction Method for Pattern Based Circuit Simulation," IEEE Custom Integrated Cir. Conf., pp. 9.4/1-9.4/4); or Chakrabarti et al. ("An Improved Hierarchical Test Generation Technique for Combinational Circuits with Repetitive Sub-Circuits," IEEE Proc. Test Symp., pp. 237-243).

The Examiner also rejected claims 9-12, 14-24, 26-36, and 38-44 under 35 U.S.C. §102(e) as being anticipated by Hachiya (U.S. Patent No. 6,031,979).

Rejections Under § 103

In the final Office Action, the Examiner rejected claims 9-12, 14-24, 26-36, and 38-44 under 35 U.S.C. §103(a) as being unpatentable over Shinsha et al. (U.S. Patent No. 4,882,690); or Wang et al. ("Restructuring Binary Decision Diagrams Based on Functional Equivalence," IEEE Design Automation, pp. 261-65); or Kuehlmann et al. ("Equivalence Checking Using Cuts and Heaps," IEEE Proc. 1997 Design Auto. Conf., pp. 263-68).

In item 18 on page 13 of the final Office Action, the Examiner indicated that the Appellant argued against the Shinsha, Wang, and Kuehlmann references individually without addressing the combination of these references when the rejection is based on a combination of references. However, the rejection in item 10 on page 7 of the final Office Action is not based on a combination of references. Rather, the rejection is based on Shinsha **or** Wang **or** Kuehlmann. Also, for a rejection based on a combination of references, the Examiner must provide motivation to combine the references. The Examiner has not provided any motivation to combine the teachings of the § 103 references. Thus, Appellant's argument below addresses the Shinsha, Wang, and Kuehlmann references individually. However, even if these references were combined, the combination of references would not realize the present invention.

The Independent Claims

Claims 9, 21, and 33 are independent claims.

Claim 9 recites a method of carrying out simulation of a circuit, including "extracting, from the circuit to be simulated, the plurality of partial circuits to inspect for equivalent operational characteristics; inspecting the plurality of partial circuits to detect partial circuits exhibiting equivalent operational characteristics, based on the configurations of the plurality of partial circuits, and judging equivalence when the configurations of said plurality of partial circuits are mutually consistent; and compressing the circuit by integrating the partial circuits exhibiting equivalent operational characteristics into one circuit and simulating the compressed circuit."

Similar to claim 9, claim 21 recites a system for carrying out simulation of a circuit, including "a circuit extracting unit extracting, from the circuit to be simulated, the plurality of partial circuits to inspect for equivalent operational characteristics; ... and a circuit equivalence inspecting unit detecting partial circuits exhibiting equivalent operational characteristics by inspecting the plurality of partial circuits on the basis of the configurations of the plurality of partial circuits, and having a judging unit judging equivalence when the configurations of said plurality of partial circuits are mutually consistent, wherein the circuit to be simulated is compressed by integrating the partial circuits exhibiting equivalent operational characteristics into one circuit and circuit simulation is performed on the compressed circuit."

Also, claim 33 recites an apparatus for carrying out simulation of a circuit, including "a circuit extracting circuit extracting, from the circuit to be simulated, the plurality of partial circuits to inspect for equivalent operational characteristics; ... and a circuit-equivalent inspecting circuit detecting partial circuits exhibiting equivalent operational characteristics by inspecting the plurality of partial circuits on the basis of the configurations of the plurality of partial circuits, and having a judging circuit judging equivalence when the configurations of said plurality of partial circuits are mutually consistent, wherein the circuit to be simulated is compressed by integrating the partial circuits exhibiting equivalent operational characteristics into one circuit and circuit simulation is performed on the compressed circuit."

The Filseth Reference

The Appellant has reviewed the large portion of the Filseth reference quoted in the final Office Action and does not find that the cited text teaches or suggests the present invention.

The Filseth reference discloses a method for flattening hierarchical design descriptions of electronic circuits by using a program called a "linker" or "flattener." The output from a linker is a flattened or expanded description of the input circuit descriptions. In Filseth, copies are created of submodule descriptions that are used more than once. This creates a flattened representation of the input hierarchical design, typically in the form of a tree structure. See Filseth, col. 1, line 6 to col. 2, line 15 and col. 3, lines 18-29. Figures 2A through 2D of Filseth illustrate the progressive expansion or flattening of the hierarchical design shown in Figs. 1A through 1D.

In Filseth, logic circuit descriptions represented hierarchically must be expanded into flat circuit descriptions to perform circuit simulation for complex logic circuits. The program "linker" or "flattener" is used in Filseth merely to expand logic circuit descriptions represented hierarchically into flat circuit descriptions to perform circuit simulation for complex logic circuits.

In Filseth, the program "linker" or "flattener" reads hierarchical descriptions of logic circuits and produces flat circuit descriptions that are enlarged in circuit size more than the hierarchical descriptions, on the presumption that the hierarchical descriptions of logic circuits cannot be used to perform circuit simulation, and that circuit simulation can be performed only by using flat logic circuits represented by the enlarged flat circuit descriptions. Consequently, dealing with LSI circuits using the method of Filseth becomes very difficult, and the time required to perform circuit simulation in Filseth using flat logic circuits increases substantially due to an enlargement of circuit size in the flat logic circuits.

In contrast, in the present invention, circuit simulation is performed using a circuit that has been compressed by integrating partial circuits exhibiting equivalent operational characteristics into one partial circuit. Thus, in the present invention, the time required to perform circuit simulation can be reduced substantially because the circuit used for circuit simulation is reduced in circuit size by integrating partial circuits exhibiting equivalent operational characteristics into one partial circuit.

Thus, it is submitted that the method of Filseth for flattening hierarchical descriptions of logic circuits using the "linker" or "flattener" program does not teach or suggest performing

circuit simulation by integrating a plurality of partial circuits, which are determined to exhibit equivalent operational characteristics, into one partial circuit.

The Yokomizo Reference

Yokomizo discloses a circuit recognition and reduction method for pattern-based circuit simulation. In Yokomizo, circuit elements extracted from layout pattern data are combined to reconstruct logic gates. Circuit data having a structure of the logic gates is recognized by the connection between gate terminals of the logic gates. The recognized circuit data are reduced by tracing signal flows and picking up the logic gates along specified critical paths. See Yokomizo at abstract.

For each simulation of the specified critical paths, only subcircuit data corresponding to the critical paths are picked up from the entire circuit data to reduce the simulated circuit size (Yokomizo at p. 9.4.1). Most potential clocked transistors determined by an additional design rule (which requires that, for the entire circuit design, either the drain terminal of the clocked transistor must be connected to the output node of the gate, or that the source terminal of the clocked transistor must be connected to the power bus node) are successively eliminated (Yokomizo at p. 9.4.2).

Thus, it is submitted that the circuit recognition and reduction method of Yokomizo, which involves extracting subcircuits along critical paths and merging or eliminating parasitic elements, does not teach or suggest performing circuit simulation by integrating a plurality of partial circuits, which are determined to exhibit equivalent operational characteristics, into one partial circuit.

The Chakrabarti Reference

The Chakrabarti reference discloses a hierarchical test pattern generation technique for combinational circuits with repetitive sub-circuits, in which the regularity of one circuit is exploited by grouping together identical gate-level sub-circuits into high-level sub-circuits based upon the characteristics of logical operations. In Chakrabarti, a hierarchical test pattern is generated at high speed using a circuit model with the high-level sub-circuits. See Chakrabarti at abstract.

In contrast, in the present invention, circuit simulation is performed by integrating a plurality of partial circuits that are determined to exhibit equivalent operational characteristics into one partial circuit.

Thus, it is submitted that the hierarchical test generation technique of Chakrabarti does not teach or suggest the circuit simulation of the present invention, in which circuit simulation is performed by integrating a plurality of partial circuits, which are determined to exhibit equivalent operational characteristics, into one partial circuit.

The Hachiya Reference

Hachiya relates to a circuit partitioning apparatus used in parallel circuit simulation to uniformly partition a target circuit prior to the execution of circuit simulation (Hachiya at col. 1, lines 8-11). In Hachiya, an input target circuit is partitioned into clusters that are collected to create a plurality of sub-circuits. Figure 5 of Hachiya illustrates initial clustering of the circuit of Fig. 4A. Simulation computation time is predicted for each sub-circuit by using a circuit matrix for each sub-circuit prior to the execution of parallel circuit simulation. Clustering is performed to create sub-circuits that require equal computation time for circuit simulation. See Hachiya at abstract.

Hachiya merges pairs of clusters. Before merging a candidate pair of clusters, the computation time prediction is used to determine the magnitude of a load after merging as the sum of the size of the two clusters. Merging is executed only if the computed value does not exceed a target magnitude. See Hachiya at col. 8, lines 62-67.

Thus, it is submitted that the circuit patterning apparatus of Hachiya that executes parallel circuit simulation does not teach or suggest performing circuit simulation by integrating a plurality of partial circuits, which are determined to exhibit equivalent operational characteristics, into one partial circuit.

The Shinsha Reference

The Shinsha reference discloses a method for automatically updating gate-level logic according to modifications of functional-level logic. See Shinsha at abstract.

In Shinsha, when new gate-level logic is produced by altering functional-level logic, the new gate-level logic that has been altered is compared with the current gate-level logic that has not been altered. Both corresponding portions (or sub-logics) that are common logically to the new gate-level logic and the current gate-level logic, and non-corresponding portions that are not common logically to the new gate-level logic and the current gate-level logic, are extracted to distinguish the corresponding portions from the non-corresponding portions. In other words, it is determined in Shinsha whether there are any corresponding portions (or sub-logics) that are common to the new gate-level logic and the current gate-level logic, only on the basis of functional-level logic.

The gate-level logic is updated using current physical design information obtained for the current gate-level logic for the corresponding portions, and also using new physical design information obtained for the non-corresponding portions. The updated gate-level logic is produced by coupling the corresponding portions that do not need to be modified with the non-corresponding portions that have been modified using the new physical design information.

In contrast, in the present invention, it is determined whether partial circuits extracted from a circuit exhibit equivalent operational characteristics based upon configurations of these partial circuits, for example, component elements of these partial circuits and the connectional relationship between these component elements. Before circuit simulation is performed, the circuit is compressed by integrating the partial circuits exhibiting equivalent operational characteristics into one circuit.

Also, Shinsha has a disadvantage in that it may be determined that two kinds of sub-logics having very different delay characteristics are common to each other. Even though two kinds of sub-logics may have the same functional-level logic, delay time of signals that are to be transferred in one sub-logic may be different from that in the other sub-logic if circuit configurations differ from each other. Consequently, it is not possible to use the method of Shinsha to perform circuit simulation by integrating partial circuits (sublogics) exhibiting equivalent operational characteristics into one partial circuit.

The present invention overcomes the disadvantage of Shinsha because it is determined in the present invention whether partial circuits extracted from a circuit exhibit equivalent operational characteristics based upon configurations of these partial circuits.

Thus, it is submitted that the method of Shinsha for automatically updating gate-level logic does not teach or suggest performing circuit simulation by integrating a plurality of partial

circuits, which are determined to exhibit equivalent operational characteristics, into one partial circuit.

The Wang Reference

The Wang reference discloses a method for restructuring Binary Decision Diagrams (BDDs) from a given input ordering to any other ordering, based on functional equivalence and structure equivalence of the BDDs. See Wang at abstract. Wang searches for common portions of different types of BDDs or combinational circuits based upon functional-level logic. Consequently, it is not possible to use the method of Wang to perform circuit simulation by integrating partial circuits (BDDs or combinational circuits) exhibiting equivalent operational characteristics into one partial circuit.

Thus, is it submitted that the method of Wang for restructuring BDDs does not teach or suggest performing circuit simulation by integrating a plurality of partial circuits, which are determined to exhibit equivalent operational characteristics, into one partial circuit.

The Kuehlmann Reference

The Kuehlmann reference discloses a method for comparing large combinational circuits with some structural similarities by using BDDs. See Kuehlmann, abstract. Kuehlmann checks the functional equivalence of combinational circuits. Similar to the Wang reference, Kuehlmann searches for common portions of different types of BDDs or combinational circuits based upon functional-level logic. Consequently, it is not possible to use the method of Kuehlmann to perform circuit simulation by integrating partial circuits (BDDs or combinational circuits) exhibiting equivalent operational characteristics into one partial circuit.

Thus, it is submitted that the method of Kuehlmann for comparing large combinational circuits with some structural similarities does not teach or suggest performing circuit simulation by integrating a plurality of partial circuits, which are determined to exhibit equivalent operational characteristics, into one partial circuit.

The Dependent Claims

The dependent claims depend from the above-discussed independent claims and are patentable over the prior art for at least the reasons discussed above.

9. CONCLUSION

In summary, it is submitted that none of the cited references teaches or suggests inspecting a plurality of extracted partial circuits to detect partial circuits exhibiting equivalent operational characteristics, based on the configurations of the plurality of partial circuits, determining equivalence when the configurations of the plurality of partial circuits are mutually consistent, and compressing the circuit to be simulated by integrating the partial circuits exhibiting equivalent operational characteristics into one circuit and simulating the compressed circuit.

Thus, Appellant submits that claims 9-12, 14-24, 26-36, and 38-44 patentably distinguish over the prior art. Accordingly, Appellant respectfully requests reversal of the Examiner's rejections.

The Commissioner is authorized to charge any Appeal Brief fee or Petition for Extension of Time fee for underpayment, or credit any overpayment, to Deposit Account No. 19-3935.

Respectfully submitted,
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10. APPENDIX ((37 C.F.R. §1.192(c)(9))

1. (CANCELLED)

2. (CANCELLED)

3. (CANCELLED)

4. (CANCELLED)

5. (CANCELLED)

6. (CANCELLED)

7. (CANCELLED)

8. (CANCELLED)

9. (THREE TIMES AMENDED) A method of carrying out simulation of a circuit, comprising:

inputting data comprising configurations for a plurality of partial circuits, and connectional relationships for input and output terminals of the partial circuits;

extracting, from the circuit to be simulated, the plurality of partial circuits to inspect for equivalent operational characteristics;

inspecting the plurality of partial circuits to detect partial circuits exhibiting equivalent operational characteristics, based on the configurations of the plurality of partial circuits, and judging equivalence when the configurations of said plurality of partial circuits are mutually consistent; and

compressing the circuit by integrating the partial circuits exhibiting equivalent operational characteristics into one circuit and simulating the compressed circuit.

10. (NOT AMENDED) The method of claim 9, wherein said inspecting the plurality of partial circuits is based on the connectional relationships of at least one of the corresponding input terminals and output terminals of the plurality of partial circuits.

11. (NOT AMENDED) The method of claim 9, wherein said inspecting the plurality of partial circuits is based on the operational characteristics of corresponding component elements of the plurality of partial circuits.

12. (NOT AMENDED) The method of claim 9, wherein the circuit to be simulated is a MOS circuit comprising a plurality of MOS semiconductor devices.

13. (CANCELLED)

14. (NOT AMENDED) The method of claim 9, further comprising judging non-equivalence when the configurations of the plurality of partial circuits are mutually inconsistent.

15. (ONCE AMENDED) The method of claim 9, further comprising assessing the intensity of influence of an external terminal of the circuit by tracing paths linking the external terminal and one or more terminals of the plurality of partial circuits.

16. (NOT AMENDED) The method of claim 15, wherein said inspecting the plurality of partial circuits is based on the intensity of the influence of the external terminal.

17. (NOT AMENDED) The method of claim 15, wherein the circuit to be simulated is a MOS circuit comprising a plurality of MOS semiconductor devices.

18. (NOT AMENDED) The method of claim 9, wherein said assessing the intensity of influence of an external terminal is determined as the frequency of shifting from the source or drain of a MOS semiconductor device to the gate thereof while tracing a path linking the external terminal and a given terminal of each of the plurality of partial circuits.

19. (NOT AMENDED) The method of claim 9, wherein when the connectional relationships of at least one of the corresponding input terminals and output terminals of the plurality of partial circuits are judged to be mutually inconsistent, a plurality of other partial circuits connected to at least one of the corresponding input terminals and output terminals are inspected for quasi-equivalent circuits, and when the plurality of other partial circuits are judged as quasi-equivalent circuits, the plurality of partial circuits are regarded as exhibiting equivalent operational characteristics.

20. (NOT AMENDED) The method of claim 9, wherein when the plurality of partial circuits are inspected for equivalence, a unique element having no counterpart within the circuit to be simulated is detected, and if a terminal that has not been judged to be a unique terminal having no counterpart is included in the terminals connected to the unique element, the terminal is newly judged to be a unique terminal, and the plurality of partial circuits connected to the newly judged unique terminal are inspected for equivalence.

21. (TWICE AMENDED) A system for carrying out simulation of a circuit, comprising:

a data input unit inputting data comprising configurations for a plurality of partial circuits, and connectional relationships for input and output terminals of the partial circuits;

a circuit extracting unit extracting, from the circuit to be simulated, the plurality of partial circuits to inspect for equivalent operational characteristics;

a storage unit holding data concerning configurations of the plurality of partial circuits; and

a circuit equivalence inspecting unit detecting partial circuits exhibiting equivalent operational characteristics by inspecting the plurality of partial circuits on the basis of the configurations of the plurality of partial circuits, and having a judging unit judging equivalence when the configurations of said plurality of partial circuits are mutually consistent,

wherein the circuit to be simulated is compressed by integrating the partial circuits exhibiting equivalent operational characteristics into one circuit and circuit simulation is performed on the compressed circuit.

22. (NOT AMENDED) The system of claim 21, wherein said storage unit holds data concerning the connectional relationships of at least one of the corresponding input terminals and output terminals of the plurality of partial circuits, and said circuit-equivalence inspecting unit detects partial circuits on the basis of the connectional relationships of at least one of the corresponding input terminals and output terminals of the plurality of partial circuits.

23. (NOT AMENDED) The system of claim 21, wherein said storage unit holds data concerning the operational characteristics of corresponding component elements of the plurality of partial circuits, and said circuit-equivalence inspecting unit detects partial circuits on the basis of the operational characteristics of corresponding component elements of the plurality of partial circuits.

24. (NOT AMENDED) The system of claim 21, wherein the circuit to be simulated is a MOS circuit comprising a plurality of MOS semiconductor devices.

25. (CANCELLED)

26. (NOT AMENDED) The system of claim 21, wherein said circuit-equivalence inspecting unit further comprises a judging unit judging non-equivalence when the configurations of the plurality of partial circuits are mutually inconsistent.

27. (ONCE AMENDED) The system of claim 21, further comprising an assessing unit assessing the intensity of influence of an external terminal of the circuit by tracing paths linking the external terminal and one or more terminals of the plurality of partial circuits.

28. (NOT AMENDED) The system of claim 27, wherein said circuit-equivalence inspecting unit detects partial circuits on the basis of the intensity of the influence of the external terminal.

29. (NOT AMENDED) The system of claim 27, wherein the circuit to be simulated is a MOS circuit comprising a plurality of MOS semiconductor devices.

30. (NOT AMENDED) The system claim 29, wherein the intensity of influence of said external terminal is determined as the frequency of shifting from the source or drain of a MOS semiconductor device to the gate thereof while tracing a path linking the external terminal and a given terminal of each of the plurality of partial circuits.

31. (NOT AMENDED) The system of claim 21, further comprising a connected-circuit quasi-equivalence inspecting unit inspecting, when said circuit-equivalence inspecting unit judges that the connectional relationship of at least one of the corresponding input terminals and output terminals of the plurality of partial circuits are mutually inconsistent, a plurality of other partial circuits connected to at least one of the corresponding input terminals and output terminals for quasi-equivalent circuits, wherein when said connected-circuit quasi-equivalence inspecting unit judges that the plurality of other partial circuits are quasi-equivalent circuits, the plurality of partial circuits are regarded as exhibiting equivalent operational characteristics.

32. (NOT AMENDED) The system of claim 21, wherein when the plurality of partial circuits are inspect for equivalence, said circuit-equivalence inspecting unit detects a unique element having no counterpart within the circuit to be simulated, and if a terminal that has not been judged to be a unique terminal having no counterpart is included in the terminals connected to the unique element, the terminal is newly judged to be a unique terminal, and the plurality of partial circuits connected to the newly judged unique terminal are inspected for equivalence.

33. (TWICE AMENDED) An apparatus for carrying out simulation of a circuit, comprising:

a data input circuit inputting data comprising configurations for a plurality of partial circuits, and connectional relationships for input and output terminals of the partial circuits;

a circuit extracting circuit extracting, from the circuit to be simulated, the plurality of partial circuits to inspect for equivalent operational characteristics;

a storage circuit holding data concerning configurations of the plurality of partial circuits; and

a circuit-equivalent inspecting circuit detecting partial circuits exhibiting equivalent operational characteristics by inspecting the plurality of partial circuits on the basis of the configurations of the plurality of partial circuits, and having a judging circuit judging equivalence when the configurations of said plurality of partial circuits are mutually consistent,

wherein the circuit to be simulated is compressed by integrating the partial circuits exhibiting equivalent operational characteristics into one circuit and circuit simulation is performed on the compressed circuit.

34. (NOT AMENDED) The apparatus of claim 33, wherein said storage unit holds data concerning the connectional relationships of at least one of the corresponding input terminals and output terminals of the plurality of partial circuits, and said circuit-equivalence inspecting unit detects partial circuits on the basis of the connectional relationships of at least one of the corresponding input terminals and output terminals of the plurality of partial circuits.

35. (NOT AMENDED) The apparatus of claim 33, wherein said storage unit holds data concerning the operational characteristics of corresponding component elements of the plurality of partial circuits, and said circuit-equivalence inspecting unit detects partial circuits on the basis of the operational characteristics of corresponding component elements of the plurality of partial circuits.

36. (NOT AMENDED) The apparatus of claim 33, wherein the circuit to be simulated is a MOS circuit comprising a plurality of MOS semiconductor devices.

37. (CANCELLED)

38. (NOT AMENDED) The apparatus of claim 33, wherein said circuit-equivalence inspecting unit further comprises a judging unit judging non-equivalence when the configurations of the plurality of partial circuits are mutually inconsistent.

39. (ONCE AMENDED) The apparatus of claim 33, further comprising an assessing unit assessing the intensity of influence of an external terminal of the circuit by tracing paths linking the external terminal and one or more terminals of the plurality of partial circuits.

40. (NOT AMENDED) The apparatus of claim 39, wherein said circuit-equivalence inspecting unit detects partial circuits on the basis of the intensity of the influence of the external terminal.

41. (NOT AMENDED) The apparatus of claim 39, wherein the circuit to be simulated is a MOS circuit comprising a plurality of MOS semiconductor devices.

42. (NOT AMENDED) The apparatus of claim 41, wherein the intensity of influence of said external terminal is determined as the frequency of shifting from the source or drain of a MOS semiconductor device to the gate thereof while tracing a path linking the external terminal and a given terminal of each of the plurality of partial circuits.

43. (NOT AMENDED) The apparatus of claim 33, further comprising a connected-circuit quasi-equivalence inspecting unit inspecting, when said circuit-equivalence inspecting unit judges that the connectional relationship of at least one of the corresponding input terminals and output terminals of the plurality of partial circuits are mutually inconsistent, a plurality of other partial circuits connected to at least one of the corresponding input terminals and output terminals for quasi-equivalent circuits,

wherein when said connected-circuit quasi-equivalence inspecting unit judges that the plurality of other partial circuits are quasi-equivalent circuits, the plurality of partial circuits are regarded as exhibiting equivalent operational characteristics.

44. (NOT AMENDED) The apparatus of claim 33, wherein when the plurality of partial circuits are inspect for equivalence, said circuit-equivalence inspecting unit detects a unique element having no counterpart within the circuit to be simulated, and if a terminal that has not been judged to be a unique terminal having no counterpart is included in the terminals connected to the unique element, the terminal is newly judged to be a unique terminal, and the plurality of partial circuits connected to the newly judged unique terminal are inspected for equivalence.

45. (CANCELLED)

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AF/ 2123
2700 #

S&H Form: (01/03)

REPLY/AMENDMENT FEE TRANSMITTAL

Attorney Docket No.	122.1329
Application Number	09/045,041
Filing Date	March 20, 1998
First Named Inventor	Hisanori FUJISAWA
Group Art Unit	2123
Examiner Name	Hugh Jones

AMOUNT ENCLOSED	430.00

FEE CALCULATION (fees effective 01/01/03)

CLAIMS AS AMENDED	Claims Remaining After Amendment	Highest Number Previously Paid For	Number Extra	Rate	Calculations
TOTAL CLAIMS	33	- 37 =	0	X $ 18.00 =	$ 0.00
INDEPENDENT *CLAIMS	3	- 4 =	0	X $ 84.00 =	0.00
Since an Official Action set an original due date of April 26, 2003, petition is hereby made for an extension to cover the date this reply is filed for which the requisite fee is enclosed (1 month ($110); 2 months ($410); 3 months ($930); 4 months ($1,450); 5 months ($1,970)):					110.00
Appeal Brief is enclosed, add ($320)					320.00
If Statutory Disclaimer under Rule 20(d) is enclosed, add fee ($110)					0.00
Total of above Calculations =					$ 430.00
Reduction by 50% for filing by small entity (37 CFR 1.9, 1.27 & 1.28)					
TOTAL FEES DUE =					$ 430.00

(1) If entry (1) is less than entry (2), entry (3) is "0".
(2) If entry (2) is less than 20, change entry (2) to "20".
(4) If entry (4) is less than entry (5), entry (6) is "0".
(5) If entry (5) is less than 3, change entry (5) to "3".

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METHOD OF PAYMENT

☒ Check enclosed as payment.

☐ Charge "TOTAL FEES DUE" to the Deposit Account No. below.

☐ No payment is enclosed and no charges to the Deposit Account are authorized at this time (unless specifically required to obtain a filing date).

GENERAL AUTHORIZATION

☒ If the above-noted "AMOUNT ENCLOSED" is not correct, the Commissioner is hereby authorized to credit any overpayment or charge any additional fees necessary to:

Deposit Account No.	19-3935
Deposit Account Name	STAAS & HALSEY LLP

☒ The Commissioner is also authorized to credit any overpayments or charge any additional fees required under 37 CFR 1.16 (filing fees) or 37 CFR 1.17 (processing fees) during the prosecution of this application, including any related application(s) claiming benefit hereof pursuant to 35 USC § 120 (e.g., continuations/divisionals/CIPs under 37 CFR 1.53(b) and/or continuations/divisionals/CPAs under 37 CFR 1.53(d)) to maintain pendency hereof or of any such related application.

SUBMITTED BY: STAAS & HALSEY LLP

Typed Name	Christine Joan Gilsdorf	Reg. No.	43,635
Signature	C. Joan Gilsdorf	Date	5/22/03

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